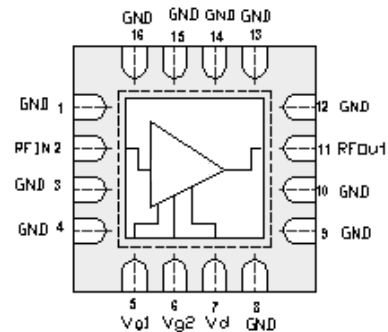


4.5 – 6 GHz Ultra Low Noise Amplifier

Features

- ◆ Frequency Range: 4.5- 6 GHz
- ◆ 1.1 dB mid band Noise Figure
- ◆ 17 dB Gain
- ◆ 10dBm Nominal P1dB @ 5.5GHz
- ◆ On-chip DC Blocks
- ◆ Bias current : 50mA (Tunable)
- ◆ 0.15-um InGaAs pHEMT Technology
- ◆ 16-Pin QFN Plastic Package : 3mmx3mmx1mm

Functional Diagram



Typical Applications

- ◆ Receiver Front End
- ◆ Military & Space
- ◆ RADAR

Description

ASL1012P3 is an Ultra Low Noise single stage Amplifier MMIC combining high gain and state of the art noise figure for Receiver Front End applications. It features 1.1dB(max) Noise Figure in 4.5 -6.0 GHz band with good I/O return Losses and 17dB gain. Input/Output matching networks, DC Blocks and bypass capacitors are provided on-chip for simplification of assembly operation. The amplifier operates on 50mA, Drain Bias of +3to+5V and Gate biases of +2.5V & -0.4 V supply. The die is fabricated using reliable Low noise 0.15um InGaAs pHEMT process. This chip is available in low cost 16 pin QFN plastic package.

Absolute Maximum Ratings¹

Parameter	Absolute Maximum	Units
Positive DC Supply	10	V
RF Input Power	20	dBm
Supply current	100	mA
Operating Temperature	-55 to +85	°C
Storage Temperature	-65 to +150	°C

1. Operation beyond these limits may cause permanent damage to the component

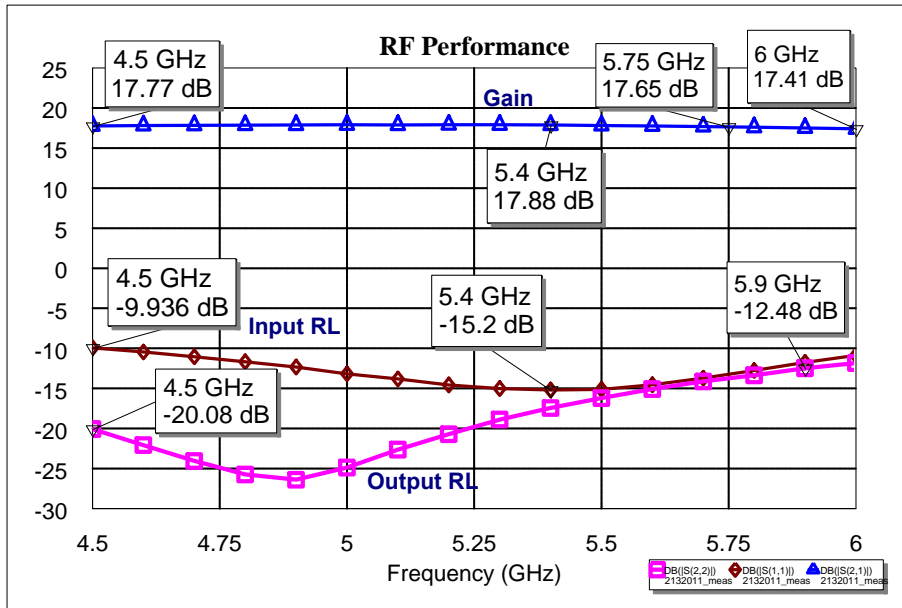
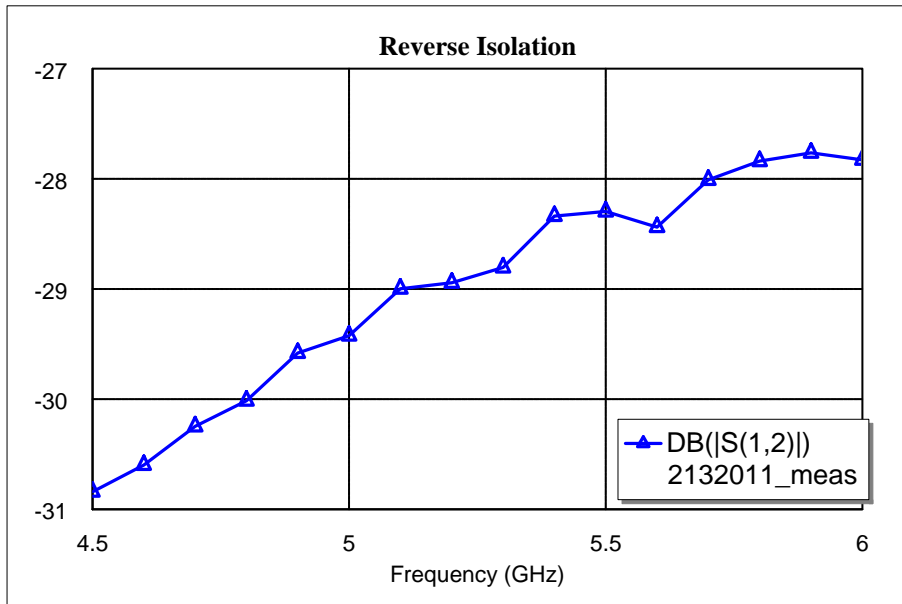
Electrical Specifications @ $T_A = 25\text{ }^\circ\text{C}$, $Z_o = 50\ \Omega$
 $V_{dd} = +4\text{V}$, $V_{g1} = -0.32\text{V}$, $V_{g2} = +2.5\text{V}$, Total Current = 50mA

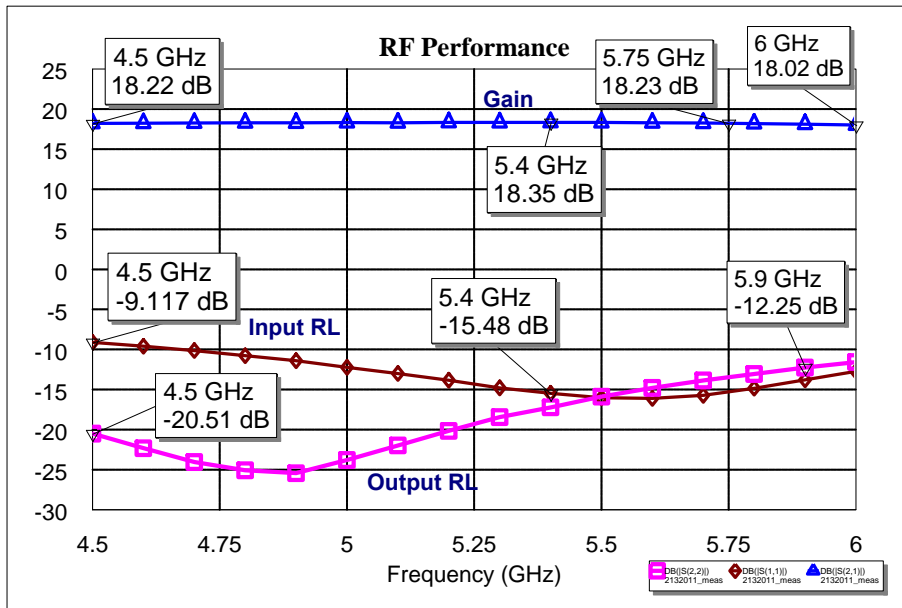
Parameter	Frequency			Units
	4.5 – 6	5.4 - 5.9	5.75 - 5.85	
Gain	17.5	17.5	17.5	dB
Gain Flatness	± 0.25	± 0.2	± 0.05	dB
Noise Figure	1.1/1.4 ⁽¹⁾	1.1/1.4 ⁽¹⁾	1.1/1.4 ⁽¹⁾	dB
Input Return Loss	-9	-12	-12	dB
Output Return Loss	-12	-12	-12	dB
Reverse Isolation	-27	-27	-27	dB
P1dB	8/12 ⁽²⁾	8/12 ⁽²⁾	8/12 ⁽²⁾	dBm
Output Third Order Intercept ⁽³⁾	25	25	25	dBm
Supply Current ⁽⁴⁾	50			mA
Bias Voltage (VD, VG1, VG2)	+4, -0.32, +2.5			V

Note:

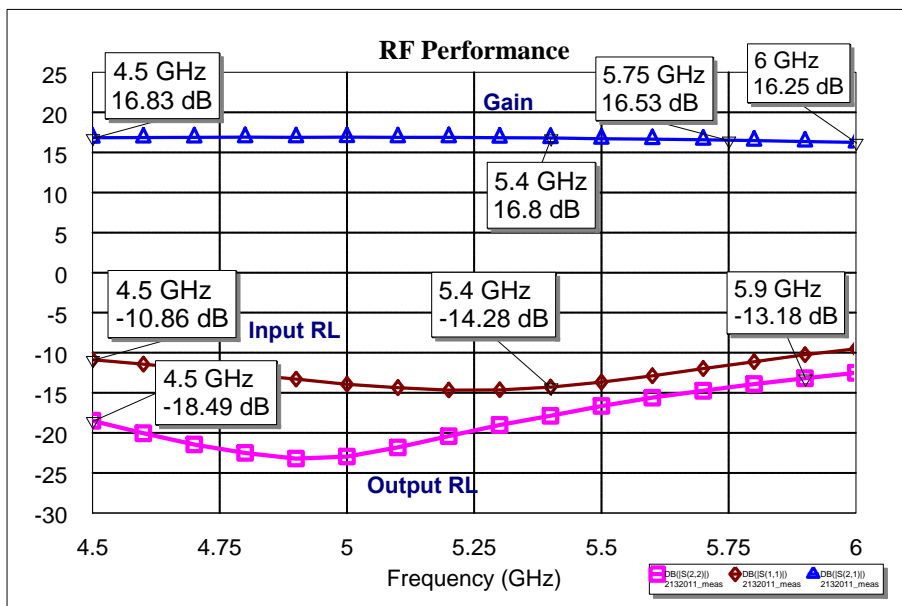
1. 1.4dB NF @ $V_d = 5\text{V}$, 50mA operation
2. 12dBm P1dB @ $V_d = 5\text{V}$
3. Estimated performance
4. VG1 can be tuned between -0.3V to -0.5V to operate the device at 50mA.
5. This is a High Performance Device. Damage can be caused due to inappropriate handling.

Test Fixture data @ $T_A = 25\text{ }^\circ\text{C}$, $Z_o = 50\text{ }\Omega$
 $V_{dd} = +4\text{V}$, $V_{g1} = -0.32\text{V}$, $V_{g2} = +2.5\text{V}$, Total Current = 50mA

RF Performance @ 4V

Reverse Isolation


Test Fixture data @ $T_A = 25\text{ }^\circ\text{C}$, $Z_o = 50\ \Omega$
RF Performance @ 3V


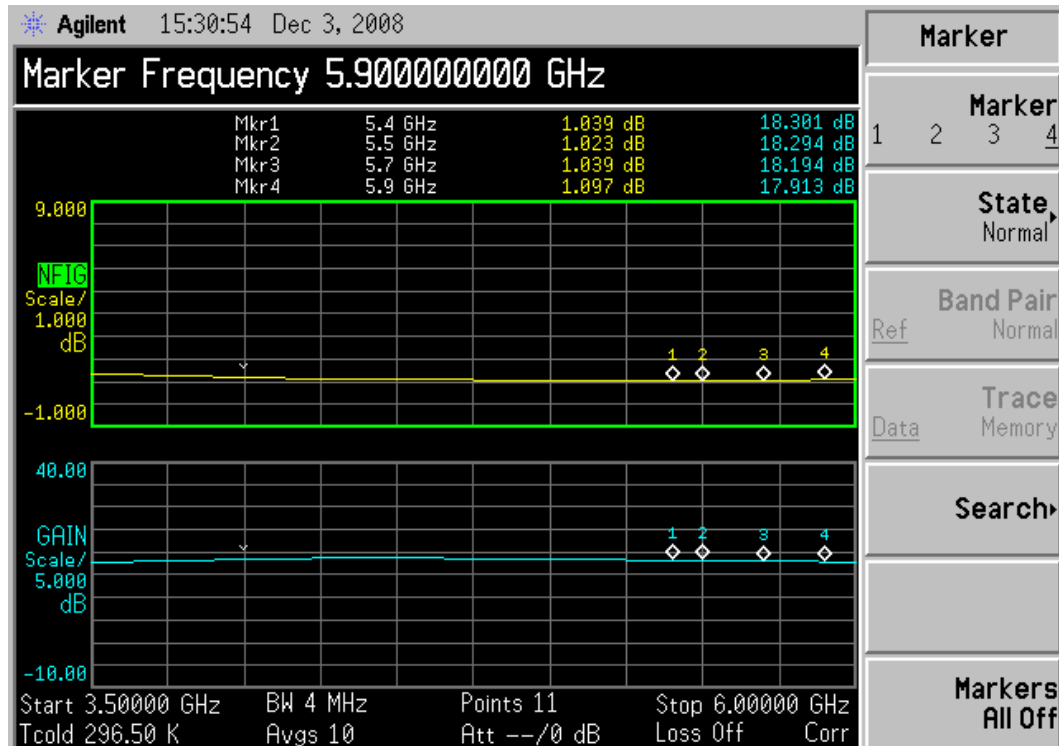
$V_{dd} = +3V$, $V_{g1} = -0.27V$, V_{g2} derived from V_{dd} , Total Current = 50mA

RF Performance @ 5V


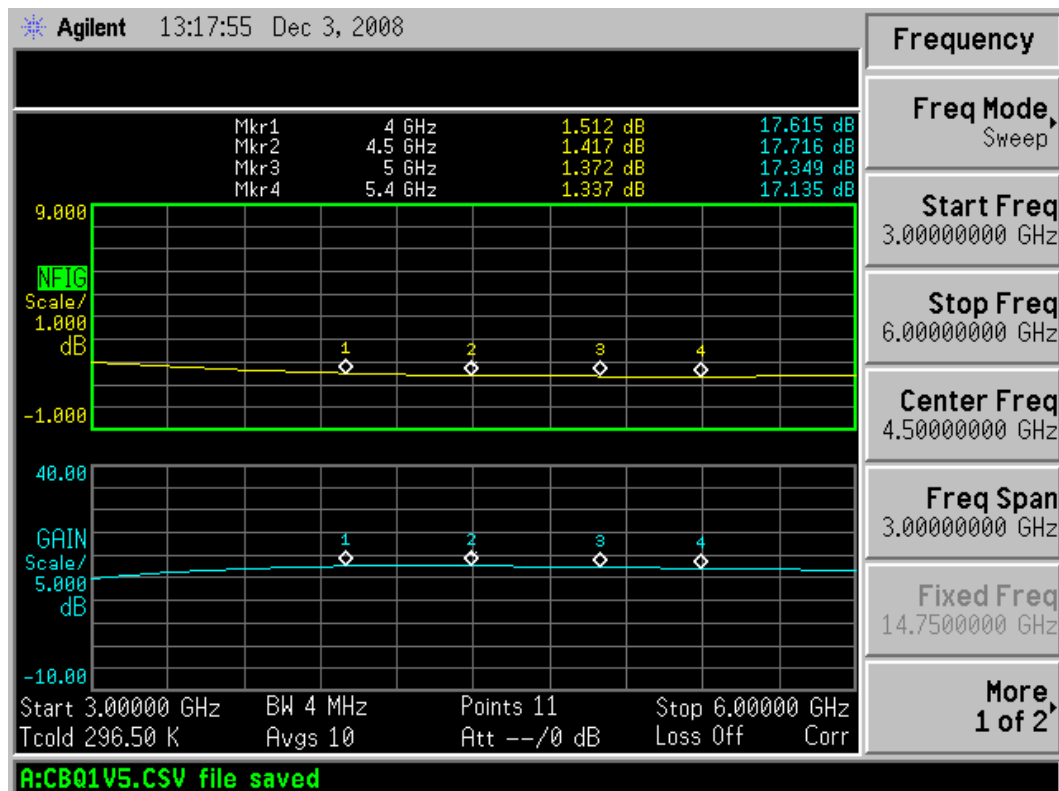
$V_{dd} = +5V$, $V_{g1} = -0.4V$, V_{g2} derived from V_{dd} , Total Current = 50mA

Test Fixture data @ $T_A = 25\text{ }^\circ\text{C}$, $Z_o = 50\ \Omega$
 Total Current = 50mA

Noise Figure @ $V_D=3V$, $I_d=50mA$

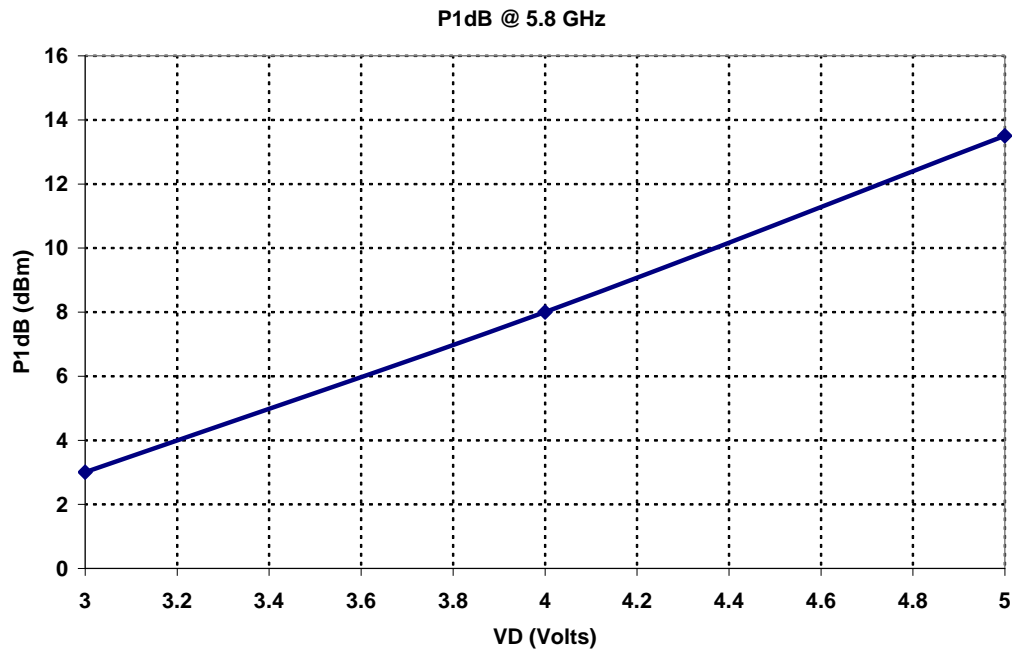


Noise Figure @ $V_D=5V$, $I_d=50mA$

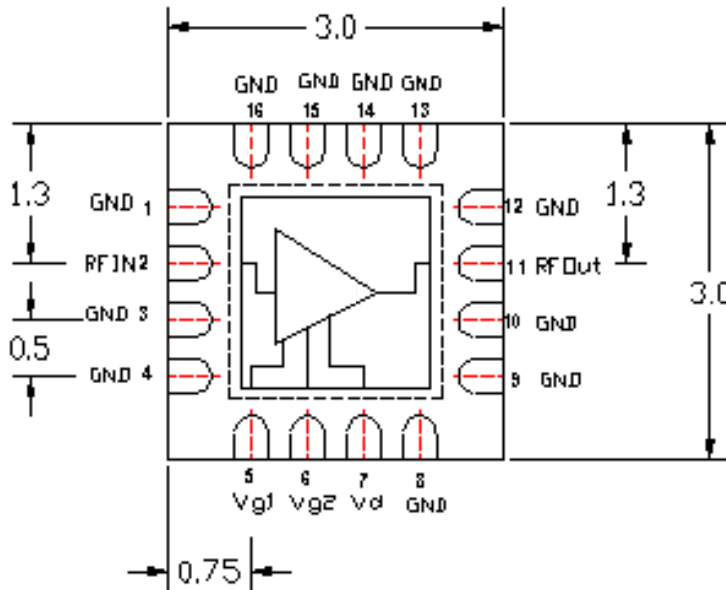


Test Fixture data @ $T_A = 25\text{ }^\circ\text{C}$, $Z_o = 50\ \Omega$

Total Current = 50mA

P1dB @ 5.8GHz Vs Drain Voltage

Mechanical Characteristics (16 Pin 3mm x 3mm x 1mm QFN Package)

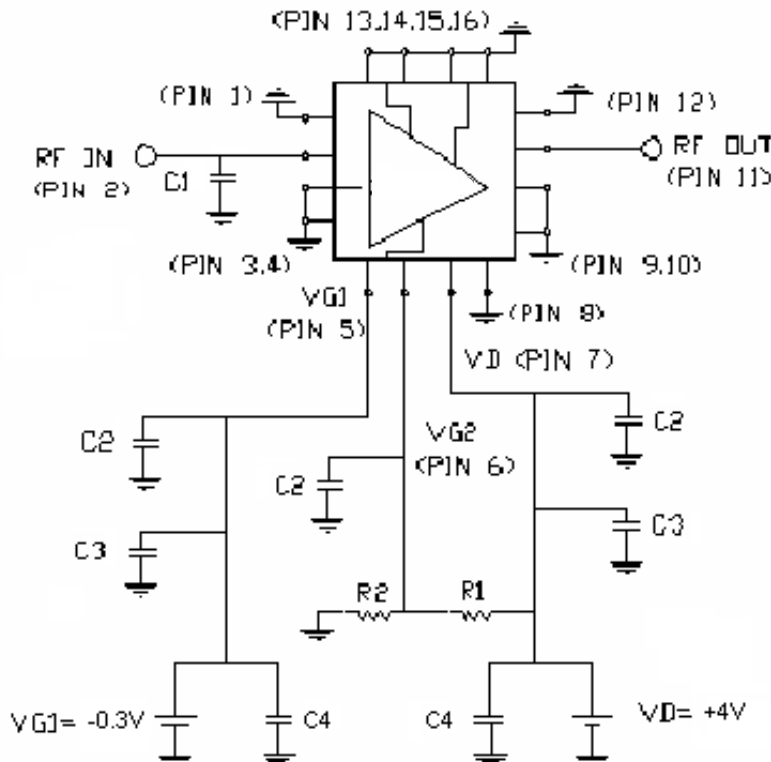


Units: millimeters

Pin Description:

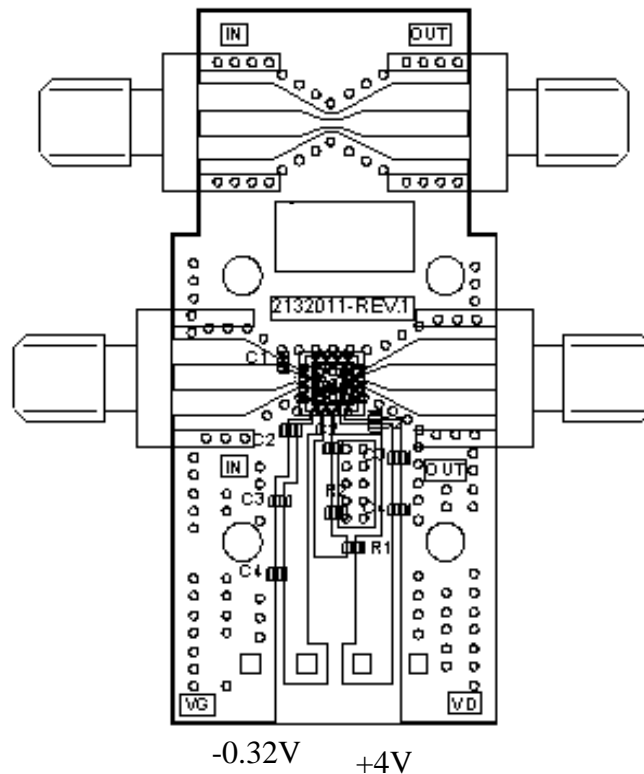
Pin 2	: RF in
Pin 5	: Gate Bias 1
Pin 6	: Gate Bias2
Pin 7	: Drain Bias
Pin11	: RF out
Pin 1,3,4,8,9,10, 12, 13,14,15,16	: Ground

Application Circuit



Note :

1. C1 is used to improve I/P match
2. C2=470pF
3. C3=0.1uF
4. C4=1uF
5. R1=4.7K, R2=8.2K

Evaluation PCB (15mm x 33mm)

List of Components

Component ID	Value	Description / Part No.
C1	0.2pF	I/P match (0603/0805 Pkg or single layer capacitor)
C2	470 pF	1 st Bypass capacitor (0402Pkg)
C3	0.1 uF	2 nd Bypass Capacitor (0402 Pkg.)
C4	1uF	2 nd Bypass Capacitor (0402 Pkg.)
R1	4.7K Ohm	Resistor in VG2 Bias network (0402 Pkg.)
R2	8.2K Ohm	Resistor in VG2 Bias network (0402 Pkg.)
Board Material : RT/Duroid 5880, 10mil		

Note:

1. Input and Output Lines should be of 50Ω Impedance.
2. Sufficient numbers of via holes should be provided for good grounding.
3. Vg2 can be applied independently without using R1 & R2 and tuned.
4. All capacitors shown in the assembly diagram are multi-layer capacitors.
5. Evaluation PCB is available from ASL upon request.



GaAs MMIC devices are susceptible to Electrostatic discharge. Proper precautions should be observed during handling, assembly & testing

All information and Specifications are subject to change without prior notice